CLAIMS

What is claimed is:

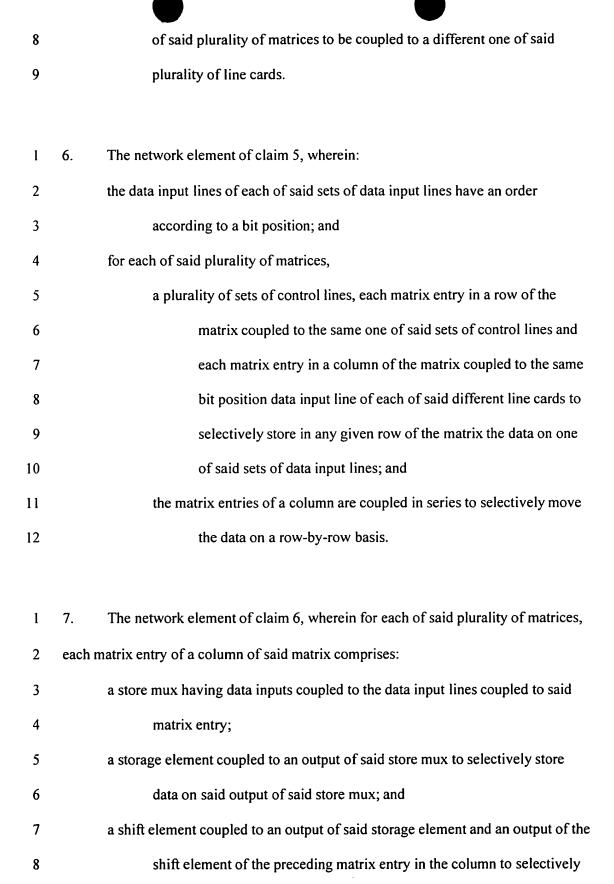
1	1. A cross-connect comprising:
2	a plurality of sets of data input lines, each of said sets of data input lines to be
3	coupled to a different line card; and
4	a plurality of matrixes each coupled to every of said set of data input lines and
5	each having a set of data output lines, the set of data input lines of each
6	of said plurality of matrices to be coupled to a different one of said line
7	cards.
1	2. The cross-connect of claim 1, wherein:
2	the data input lines of each of said sets of data input lines have an order
3	according to a bit position; and
4	for each of said plurality of matrices,
5	a plurality of sets of control lines, each matrix entry in a row of the
6	matrix coupled to the same one of said sets of control lines and
7	each matrix entry in a column of the matrix coupled to the same
8	bit position data input line of each of said different line cards to
9	selectively store in any given row of the matrix the data on one
10	of said sets of data input lines; and
11	the matrix entries of a column are coupled in series to selectively move
12	the data on a row-by-row basis.

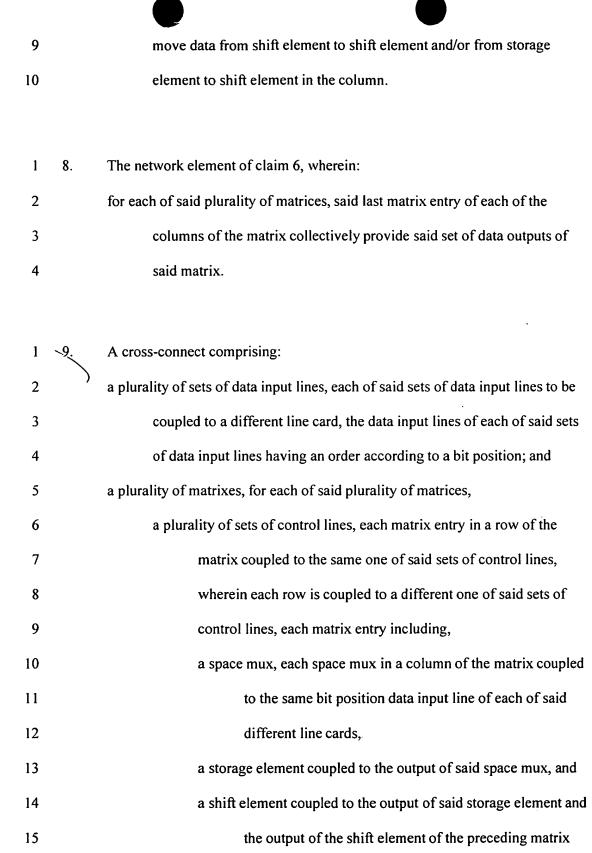
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1	3.	The cross-connect of claim 2, wherein for each of said plurality of matrices,
2	each r	matrix entry of a column of said matrix comprises:
3		a store mux having data inputs coupled to the data input lines coupled to said
4		matrix entry;
5		a storage element coupled to an output of said store mux to selectively store
6		data on said output of said store mux; and
7		a shift element coupled to an output of said storage element and an output of the
8		shift element of the preceding matrix entry in the column to selectively
9		move data from shift element to shift element and/or from storage
10		element to shift element in the column.
1 2	4.	The cross-connect of claim 2, wherein: for each of said plurality of matrices, said last matrix entry of each of the
3		columns of the matrix collectively provide said set of data outputs of
4		said matrix.
1	5.	A network element comprising:
2		a plurality of line cards; and
3		a cross-connect including a plurality of sets of data input lines, each of said sets
4		of data input lines coupled to a different one of said plurality line cards;
5		and
6		a plurality of matrixes each coupled to every of said set of data input lines and

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each having a set of data output lines, the set of data input lines of each





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entry in the same column.

1	10.	The cross-connect of claim 9, wherein said storage element of a first of said
2	matrix	entries comprises:
3		a store register having an input and an output, said output of said store register
4		coupled to said shift element of said first matrix entry; and
5		a timing mux having a data input coupled to the output of said space mux, a
6		data input coupled to the output of said store register, a control input
7		coupled to said set of control lines, and an output coupled to the input of
8		said store register.
1	11.	The cross-connect of claim 10, wherein said shift element of said first of said
2	matrix	entries comprises:
3		a shift register having an input and an output, said output of said shift register
4		providing said output of said shift element; and
5		a shift mux having a data input coupled to the output of the store register of said
6		first matrix entry, a data input coupled to the output of the shift element
7		of the preceding matrix entry in the same column, a control input
8		coupled to said set of control lines, and an output coupled to the input of
9		said shift register.
1	12.	The cross-connect of claim 9, wherein said shift element of a first of said matrix
2	entries	s comprises:
3		a shift register having an input and an output, said output of said shift register
4		providing said output of said shift element; and

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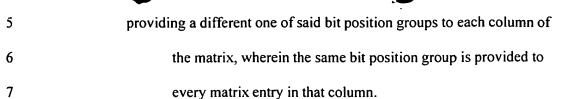
5		a shift mux having a data input coupled to the output of the storage element of
6		said first matrix entry, a data input coupled to the output of the shift
7		element of the preceding matrix entry in the same column, and a control
8		input coupled to said set of control lines, and an output coupled to the
9		input of said shift register.
1	13.	The cross-connect of claim 9, wherein:
2		for each of said plurality of matrices, said last matrix entry of each of the
3		columns of the matrix collectively provide an output of said matrix; and
4		the output of each of said plurality of matrixes is coupled to a different one of
5		said line cards.
1	14.	The cross-connect of claim 9, wherein:
2		for each of said plurality of matrices, the set of control lines for each row of the
3		matrix control said store muxes and storage elements to selectively store
4		in any given row on a row-by-row basis data from any one of said
5		different line card.
1	15.	The cross-connect of claim 9, wherein:
2		for each of said plurality of matrices, the set of control lines for each row of the
3		matrix control said shift elements to move data on a row-by-row basis in
4		said matrix.

2	a plurality of sets of data input lines, each of said sets of data input lines to be
3	coupled to a different line card;
4	a plurality of matrix means, each matrix means coupled to all of said sets of data
5	input lines to selectively store, reorder, and intermix data from said
6	different line cards, each matrix means having a output coupled to a
7	different one of said lines cards.

1	17.	A method comprising:
2)	providing on given intervals to each of a plurality of matrices a plurality of
3		ordered bits from every one of a plurality of different line cards;
4		for each of said plurality of matrices,
5		selectively storing on given intervals in any given row of the matrix the
6		plurality of ordered bits from one of said plurality of different
7		line cards, wherein said rows are coupled in series, and
8		selectively moving on given intervals data in one row of the matrix to a
9		next row in the series; and
10		providing on given intervals to each of said plurality of different line cards the
11		plurality of ordered bits from the last row of a different one said
12		plurality of matrices.

- 18. The method of claim 17, wherein:
- 2 the bits in the same bit positions according to said order from each of said
- 3 plurality of different line cards are groups into bit position groups; and
- 4 said selectively storing includes:

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- 1 19. The method of claim 17, wherein said selectively storing and said selectively
- 2 moving further comprises:
- providing a different set of control signals to each row of the matrix, wherein
- 4 the set of control signals is provided to every matrix entry in that row.